Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A protection circuit associated with a first transistor of a voltage specification of a first voltage level, said first transistor and said protection circuit being comprised in an integrated circuit designed to process information in an input signal having a swing equaling a second voltage level, wherein said first voltage level is lower than said second voltage level, said protection circuit comprising: a second PMOS transistor which switches to an off state if said input signal having said swing would cause a cross terminal voltage of said first transistor to exceed a permissible range, wherein said second PMOS transistor in said off state ensures that said cross terminal voltage of said first transistor does not exceed said permissible range.

[c2] 2. The protection circuit of claim 1, wherein said first transistor comprises a first PMOS transistor.

[c3] 3. The protection circuit of claim 2, wherein a source terminal of said first PMOS transistor being connected to a supply voltage of said second voltage level.

[c4] 4. The protection circuit of claim 3, wherein said input

signal swings between a reference voltage and said second voltage level.

[c5] 5. The protection circuit of claim 2, wherein said integrated circuit further comprises a first NMOS transistor also of said voltage specification of said first voltage level, said protection circuit further comprising:
a second NMOS transistor which switches to an off state if said input signal would cause a cross terminal voltage of said first NMOS transistor to exceed a permissible range, wherein said second NMOS transistor in said off state ensures that said cross terminal voltage of said first NMOS transistor does not exceed said permissible range.

[c6] 6. The protection circuit of claim 5, wherein an upper limit of said permissible range equals an allowed maximum voltage associated with each of said first PMOS transistor and said first NMOS transistor.

[c7] 7. The protection circuit of claim 5, wherein each of said first PMOS transistor and said first NMOS transistor is contained in an input buffer, a drain terminal of each of said second PMOS transistor and said second NMOS transistor being coupled to receive said input signal, a gate terminal of said second PMOS transistor being connected to receive a first bias voltage and a gate terminal

of said second NMOS transistor being connected to receive a second bias voltage.

[c8] 8. The protection circuit of claim 7, said protection circuit further comprising:
a third PMOS transistor, a gate terminal of said third PMOS transistor being connected to said first bias voltage, a source terminal of said third PMOS transistor being connected to a gate terminal of said first PMOS transistor,
a drain terminal of said first PMOS transistor being connected to a source terminal of said second PMOS transistor, and a source terminal of said first PMOS transistor being connected to a supply voltage of said second voltage level,
wherein said third PMOS transistor ensures that a gate to source voltage (Vgs) and a gate to drain voltage (Vgd) of said first PMOS transistor from being exposed to voltage exceeding said permissible range.

[c9] 9. The protection circuit of claim 8, wherein said input buffer further comprises a fourth PMOS transistor, a gate terminal of said fourth PMOS transistor being connected to said source terminal of said second PMOS transistor, a drain terminal of said fourth PMOS transistor connected to said source terminal of said third PMOS transistor, and a source terminal of said fourth PMOS transistor being

connected to said supply voltage.

[c10] 10. The protection circuit of claim 9, wherein all of said first PMOS transistor, said second PMOS transistor, said third PMOS transistor, and said fourth PMOS transistor are of said voltage specification of said first voltage level.

[c11] 11. The protection circuit of claim 6, said protection circuit further comprising:
a third NMOS transistor, a gate terminal of said third NMOS transistor being connected to said second bias voltage, a source terminal of said third NMOS transistor being connected to a gate terminal of said first NMOS transistor,
a drain terminal of said first NMOStransistor being connected to a source terminal of said second NMOS transistor, and a source terminal of said first NMOStransistor being connected to a reference voltage,
wherein said third NMOS transistor ensures that a gate to source voltage (Vgs) and a gate to drain voltage (Vgd) of said first NMOStransistor from being exposed to voltage exceeding said permissible range.

[c12] 12. The protection circuit of claim 11, wherein said input buffer further comprises a fourth NMOS transistor, a gate terminal of said fourth NMOS transistor being connected

to said source terminal of said second NMOS transistor, a drain terminal of said fourth NMOS transistor connected to said source terminal of said third NMOS transistor, and a source terminal of said fourth NMOS transistor being connected to said reference voltage.

[c13] 13. The protection circuit of claim 12, wherein all of said first NMOStransistor, said second NMOS transistor, said third NMOS transistor, and said fourth NMOS transistor are of said voltage specification of said first voltage level.

[c14] 14. The protection circuit of claim 6, said first PMOS transistor and said first NMOS transistor being comprised in a logic gate, wherein each of said first NMOS transistor, said first PMOS transistor, said second NMOS transistor and said second PMOS transistor comprises a drain terminal, a source terminal and a gate terminal, a gate terminal of said first NMOS transistor receiving a first swing signal and a gate terminal of said first PMOS transistor receiving a second swing signal, wherein each of said first swing signal and said second swing signal has a lower swing compared to a swing of said input signal but representing said information in said input signal,

wherein said gate terminal of said second PMOS transistor is connected to a BIASP voltage, and said gate termi-

nal of said second NMOS transistor is connected to a BIASN voltage,

said source terminal of said second PMOS transistor is connected to said drain terminal of said first PMOS transistor,

said source terminal of said first PMOS transistor is connected to a supply voltage of said second voltage level,

said drain terminal of said second PMOS transistor is connected to said drain terminal of said second NMOS transistor,

said source terminal of said second NMOS transistor is connected to said drain terminal of said first NMOS, and said source terminal of said first NMOS is connected to a reference voltage.

[c15] 15. The protection circuit of claim 14, wherein the drain terminal of said first PMOS transistor provides a first output signal having a swing equal to a swing of said first swing signal, the drain terminal of said first NMOS transistor provides a second output signal having a swing equal to a swing of said second swing signal, and the drain terminal of said second NMOS transistor provides a third output signal having a swing equal to a swing of said input signal, wherein each of said first output signal, said second output signal and said third output signal represents an output of said logic gate.

[c16] 16. The protection circuit of claim 15, wherein said logic gate comprises an inverter.

[c17] 17. The protection circuit of claim 15, wherein said logic gate comprises a plurality of NMOS transistors including said first NMOS transistor, said logic gate also comprising a plurality of PMOS transistors including said first PMOS transistor, wherein a number of transistors in each of said plurality of NMOS transistors and said plurality of PMOS transistors equals a number of inputs to said logic gate.

[c18] 18. An integrated circuit processing an input signal of a first voltage level using transistors having a voltage specification of a second voltage level, wherein said first voltage level is higher than said second voltage level, said integrated circuit comprising:
a first transistor of said voltage specification, said first transistor comprising a gate terminal, a source terminal and a drain terminal; and
a second transistor comprising a gate terminal, a drain terminal and a source terminal,
a third transistor comprising a gate terminal, a source terminal and a drain terminal, wherein one of said drain terminal and said source terminal of said second transistor is connected to receive said input signal, and the

other one of said drain terminal and said source terminal of said second transistor is connected to said drain terminal of said first transistor, wherein said gate terminal of said second transistor is connected to receive a first bias voltage,

wherein the gate terminal of said third transistor is connected to said first bias voltage, said source terminal of said third transistor is connected to said gate terminal of said first transistor,

whereby said second transistor and said third transistor together ensure that said first transistor receives said input signal with a voltage level at less than said first voltage level.

[c19] 19. The integrated circuit of claim 18, wherein each of said second transistor and said third transistor is also of said voltage specification of said second voltage level.

[c20] 20. The integrated circuit of claim 18, wherein each of said first transistor, said second transistor and said third transistor comprises a PMOS transistor, and the source terminal of said first transistor is coupled to a supply voltage of said first voltage level.

[c21] 21. The integrated circuit of claim 18, wherein each of said first transistor, said second transistor and said third transistor comprises a NMOS transistor, and the source

terminal of said first transistor is coupled to a reference voltage.

[c22] 22. An integrated circuit comprising:
an input buffer comprising a plurality of transistors of a voltage specification of a first voltage level, said input buffer operating from a supply voltage,
said input buffer being operable to process an input signal of a second voltage level if said supply voltage equals said second voltage level, and to process said input signal of a third voltage level if said supply voltage equals said third voltage level, wherein each of said second voltage level and said third voltage level is greater than said first voltage level.

[c23] 23. The integrated circuit of claim 22, further comprising a protection circuit in turn comprising a second plurality of transistors,
wherein said protection circuit ensures that cross terminal voltages across each of said plurality of transistors is below an allowed maximum voltage level,
wherein each of said second plurality of transistors is also of said voltage specification.

[c24] 24. An integrated circuit comprising:
a first buffer containing a first plurality of transistors,
said first buffer receiving a first supply voltage and pro-

cessing a first input signal of a first voltage level to generate a first output signal;

a second buffer containing a second plurality of transistors, said second buffer receiving a second supply voltage and processing a second input signal of a second voltage level to generate a second output signal, wherein said second supply voltage is not equal to said first input voltage,

all of said first plurality of transistors and said second plurality of transistors being of a same voltage specification and said same voltage specification being lower than each of said first voltage level and said second voltage level; and

a core module processing said first output signal and said second output signal.

[c25] 25. The integrated circuit of claim 24, wherein said core module containing a third plurality of transistors of a different voltage specification.

[c26] 26. The integrated circuit of claim 24, wherein said core module containing a third plurality of transistors also of said same voltage specification.

[c27] 27. An input buffer receiving an input of a first voltage level, said input buffer comprising:

a first transistor and a second transistor operating as a

first inverter;

a third transistor and a fourth transistor operating as a second inverter, wherein each of said first transistor, said second transistor, said third transistor and said fourth transistor is of a voltage specification of a second voltage level, wherein said second voltage level is lower than said first voltage level; and

a protection circuit comprising a fifth transistor, a sixth transistor, a seventh transistor and a eighth transistor, wherein each of said first transistor, said second transistor, said third transistor, said fourth transistor, said fifth transistor, said sixth transistor, said seventh transistor, and said eighth transistor contains a source terminal, a drain terminal, and a gate terminal,

the drain terminal of each of said fifth transistor and said sixth transistor are connected to receive said input of said first voltage level,

the source terminal of said sixth transistor is connected to the drain terminal of said second transistor and the gate terminal of said fourth transistor at a first node,

the gate terminal of each of said sixth transistor and said eighth transistor is connected to a first bias voltage,

the source terminal of each of said second transistor and said fourth transistor is connected to receive a reference voltage,

the drain terminal of said fourth transistor is connected

to the source terminal of said eighth transistor and the gate terminal of said second transistor at a second node,
the drain terminal of said eighth transistor is connected to the drain terminal of said seventh transistor,
the gate terminal of each of said fifth transistor and said seventh transistor is connected to receive a second bias voltage,
the source terminal of said fifth transistor is connected to the drain terminal of said first transistor and the gate terminal of said third transistor at a third node,
the source terminal of said seventh transistor is connected to the drain terminal of said third transistor and the gate terminal of said first transistor at a fourth node, and
the bulk terminal of each of said first transistor, said third transistor is connected to the corresponding source terminal.

[c28] 28. The input buffer of claim 27, wherein the bulk terminal of each of said fifth transistor and said seventh transistor is connected to the corresponding source terminal.

[c29] 29. The input buffer of claim 27, wherein the bulk terminal of each of said fifth transistor and said seventh transistor is connected to said first voltage level.

[c30] 30. The input buffer of claim 27, wherein the source ter-

minal of each of said first transistor and said third transistor is connected to receive a supply voltage of said first voltage level.

[c31] 31. The input buffer of claim 30, wherein each of said first transistor, said third transistor, said fifth transistor and said seventh transistor comprises a PMOS transistor, and each of said second transistor, said fourth transistor, said sixth transistor and said eighth transistor comprises a NMOS transistor.

[c32] 32. The input buffer of claim 31, wherein each of said first bias voltage and said second bias voltage approximately equals half of said first voltage level.

[c33] 33. The input buffer of claim 32, wherein said fourth node provides a first intermediate signal which transitions between said first voltage level and (said second bias voltage plus a threshold voltage of said seventh transistor), said second node provides a second intermediate signal which transitions between said reference voltage and (said first bias voltage less a threshold voltage of said eighth transistor), and the drain terminal of said seventh transistor provides a third intermediate signal having a swing equal to a swing of said first input signal, wherein each of said first intermediate signal, said second intermediate signal and said third interme-

diate signal represents an intermediate output of said input buffer.

[c34] 34. The input buffer of claim 32, further comprising a level shifter receiving an intermediate output signal from one of said first inverter and said second inverter, and shifting a voltage level of said intermediate output signal to a third voltage level, wherein said third voltage level is lower than said first voltage level.

[c35] 35. The input buffer of claim 32, further comprising a counter_leakage circuit comprising a second NMOS transistor having a drain terminal connected to said first voltage level, a source terminal connected to said third node, and a gate terminal connected to receive a third bias voltage, wherein said third bias voltage is designed to turn on said second NMOS transistor if voltage at said third node is below (said third bias voltage less a threshold voltage of said second NMOS transistor), whereby any leakage in said fifth transistor in an off state is countered by current flow through said second NMOS transistor.

[c36] 36. The input buffer of claim 32, further comprising a counter_leakage circuit comprising a second PMOS transistor having a drain terminal connected to said reference voltage, a source terminal connected to said first

node, and a gate terminal connected to receive a fourth bias voltage, wherein said fourth bias voltage is designed to turn on said second PMOS transistor if voltage at said first node is above (said fourth bias voltage plus a threshold voltage of said second PMOS transistor), whereby any leakage in said sixth transistor in an off state is countered by current flow through said second PMOS transistor.

[c37] 37. The input buffer of claim 32, further comprising a counter_leakage circuit comprising:
a second NMOS transistor having a source terminal connected to said third node and a gate terminal connected to receive a third bias voltage, wherein said third bias voltage is designed to turn on said second NMOS transistor if voltage at said third node is below (said third bias voltage less a threshold voltage of said second NMOS transistor); and
a current amplifier connected to a drain terminal of said second NMOS transistor, wherein said current amplifier amplifies a current flowing through said second NMOS transistor, whereby any leakage in said fifth transistor in an off state is countered by current flow through said current amplifier.

[c38] 38. The input buffer of claim 32, further comprising a counter_leakage circuit comprising:

a second PMOS transistor having a source terminal connected to said first node and a gate terminal connected to receive a fourth bias voltage, wherein said fourth bias voltage is designed to turn on said second PMOS transistor if voltage at said first node is above (said fourth bias voltage plus a threshold voltage of said second PMOS transistor); and

a current amplifier connected to a drain terminal of said second PMOS transistor, wherein said current amplifier amplifies a current flowing through said second PMOS transistor, whereby any leakage in said sixth transistor in an off state is countered by current flow through said current amplifier.

[c39] 39. The input buffer of claim 32, further comprising a counter_leakage circuit comprising a second PMOS transistor having a drain terminal connected to said third node, each of a source terminal and a gate terminal connected to said first voltage level, whereby said second PMOS transistor is permanently in an off state and draws current proportionate to a difference of a voltage at said third node and said first voltage level.

[c40] 40. The input buffer of claim 32, further comprising a counter_leakage circuit comprising a second NMOS transistor having a drain terminal connected to said first node, each of a source terminal and a gate terminal con-

nected to said reference voltage, whereby said second NMOS transistor is permanently in an off state and draws current proportionate to a difference of a voltage at said first node and said reference voltage.

[c41] 41. The input buffer of claim 32, further comprising a counter_leakage circuit comprising a set of transistors connected in series, wherein a drain terminal of each of said set of transistors is connected to a gate terminal of the same transistor, and a drain terminal of a first one of said set of transistors is connected to a fifth node, said counter_leakage circuit being designed to counter leakage at said fifth node.

[c42] 42. The input buffer of claim 41, wherein said fifth node comprises one of said third node and said fourth node, wherein each of said set of transistors comprises a PMOS transistor, and a source terminal of a last one of said set of transistors is connected to said first voltage level.

[c43] 43. The input buffer of claim 40, wherein said fifth node comprises one of said first node and said second node, wherein each of said set of transistors comprises a NMOS transistor, and a source terminal of a last one of said set of transistors is connected to said reference voltage.

[c44] 44. The input buffer of claim 31, further comprising a

level shifter to shift a voltage level of an intermediate signal available at either said second node or said fourth node to a desired voltage level, said level shifter comprising:

a ninth transistor, a tenth transistor, a eleventh transistor, a twelfth transistor, and a thirteenth transistor, each comprising a source terminal, a drain terminal and a gate terminal,

the gate terminal of said ninth transistor being connected to receive said intermediate signal,

the source terminal of said ninth transistor being connected to the source terminal of said tenth transistor,

the drain terminal of said tenth transistor being connected to the drain terminal of said eleventh transistor and the gate terminal of said twelfth transistor,

the gate terminal of said tenth transistor being connected to a supply voltage providing said desired voltage level,

the drain terminal of said twelfth to the drain terminal of said thirteenth transistor and the gate terminal of said eleventh transistor,

the source terminal of each of said eleventh transistor and said twelfth transistor being connected to said supply voltage providing said desired voltage level, and

the drain terminal of said ninth transistor and source terminal of said thirteenth transistor being connected to

said reference voltage.

[c45] 45. The input buffer of claim 31, wherein a width to length (W/L) ratio of said first transistor and said fifth transistor is increased to increase a lower hysteresis threshold voltage (VIL) and a W/L ratio of said second transistor and said sixth transistor is increased to increase a higher hysteresis threshold voltage (VIH).

[c46] 46. The input buffer of claim 45, further comprising a resistor having a first end coupled to receive said input signal and another end connected to the drain terminal of said fifth transistor, said resistor being designed to provide hysteresis.

[c47] 47. The input buffer of claim 27, wherein said first transistor, said second transistor, said third transistor, said fourth transistor, said fifth transistor, said sixth transistor, said seventh transistor, and said eighth transistor are all of the same voltage specification.

[c48] 48. A combinatorial logic block performing a logic operation using a first input signal, said first input signal being either at a reference voltage to represent one logic value or a first voltage level to represent another logic value, said combinatorial logic block comprising:
a plurality of transistors coupled to perform said logic

operation using said first input signal, each of said plurality of transistors is of a voltage specification of a second voltage level, wherein said second voltage level is less than a swing of said input signal, wherein said swing equals a difference of said reference voltage and said first voltage level; and

a protection circuit preventing voltages exceeding an allowed maximum voltage from being applied across any of said plurality of transistors.

[c49] 49. The combinatorial logic block of claim 48, wherein said plurality of transistors comprise a set of PMOS transistors and a set of NMOS transistors,

said protection circuit comprising a first NMOS transistor and a first PMOS transistor,

each of said first NMOS transistor, said first PMOS transistor, said set of PMOS transistors and said set of NMOS transistors containing a source terminal, a drain terminal and a gate terminal,

the source terminal of at least one of said set of PMOS transistors being coupled to a supply voltage and the source terminal of at least one of said set of NMOS terminals being coupled to said reference voltage,

wherein the source terminal of said first PMOS transistor is connected to the drain terminal of at least one of said set of PMOS transistors, and

wherein the source terminal of said first NMOS transistor is connected to the drain terminal of at least one of said set of NMOS transistors.

[c50] 50. The combinatorial logic block of claim 49, wherein the drain terminal of said first PMOS transistor is connected to the drain terminal of said first NMOS transistor, and
the gate terminal of said first PMOS transistor is connected to a first bias voltage and the gate terminal of said first NMOS transistor is connected to a second bias voltage.

[c51] 51. The combinatorial logic block of claim 50, wherein each of said first bias voltage and said second bias voltage approximately equals half of said first voltage level.

[c52] 52. The combinatorial logic block of claim 50, further comprising a swing split circuit receiving said first input signal and generating a first swing signal and a second swing signal, each of first swing signal and said second swing signal having a lower swing compared to a swing of said first input signal, said first swing signal being connected to the gate terminal of at least one of said set of PMOS transistors and said second swing signal being connected to the gate terminal of at least one of said set of NMOS transistors.

[c53] 53. The combinatorial logic block of claim 52, wherein each of said first swing signal and said second swing signal comprises an inverted signal of said first input signal.

[c54] 54. The combinatorial logic block of claim 52, said first swing signal having a first high voltage level and a first low voltage level, and said second swing signal having a second high voltage level and a second low voltage level, wherein said first high voltage level equals said first voltage level and said second low voltage level equals said reference voltage, and wherein each of said first low voltage level and said second high voltage level substantially equal half of a difference of said first high voltage level and said reference voltage.

[c55] 55. The combinatorial logic block of claim 54, wherein the drain terminal of one of said set of PMOS transistors provides a first output signal having a swing equal to a swing of said first swing signal, the drain terminal of one of said set of NMOS transistors provides a second output signal having a swing equal to a swing of said second swing signal, and the drain terminal of said first NMOS transistor provides a third output signal having a swing equal to a swing of said first input signal, wherein each of said first output signal, said second output signal and

said third output signal represents an output of said logic operation.

[c56] 56. The combinatorial logic block of claim 55, wherein said logic operation comprises an inversion operation, and wherein each of said set of NMOS transistors and said set of PMOS transistors comprises a single transistor.

[c57] 57. The combinatorial logic block of claim 55, wherein said logic operation comprises a N_input logical operation, and wherein each of said set of PMOS transistors and said set of NMOS transistors comprises N_transistors.

[c58] 58. The combinatorial logic block of claim 54, wherein said set of PMOS transistors, said set of NMOS transistors, said first NMOS transistor, and said first PMOS transistor are all implemented of the same voltage specification.

[c59] 59. A counter_leakage circuit countering a leakage current, wherein said leakage current otherwise causes a voltage at a node to go beyond a desired voltage level, said counter_leakage circuit comprising:
a transistor having a source terminal connected to said node, and a gate terminal connected to receive a bias

voltage, wherein said bias voltage is designed to turn on said transistor if the voltage at said node goes beyond said desired voltage level, whereby any leakage at said node is countered by current flow through said transistor.

[c60] 60. The counter_leakage circuit of claim 59, wherein said transistor is of a voltage specification of a second voltage level and said transistor is operated in an environment operating with input signals of a first voltage level, wherein said first voltage level is greater than said second voltage level.

[c61] 61. The counter_leakage circuit of claim 60, wherein said transistor comprises an NMOS transistor having a drain terminal connected to said first voltage level and said NMOS transistor turns on if the voltage at said node is below (said bias voltage less a threshold voltage of said NMOS transistor).

[c62] 62. The counter_leakage circuit of claim 61, wherein said transistor comprises a PMOS transistor having a drain terminal connected to a reference voltage level and said PMOS transistor turns on if the voltage at said node is above (said bias voltage plus a threshold voltage of said PMOS transistor).

[c63] 63. A counter_leakage circuit countering a leakage current, wherein said leakage current otherwise causes a voltage at a node to go beyond a desired voltage level, said counter_leakage circuit comprising:
a PMOS transistor having a drain terminal connected to said node, each of a source terminal and a gate terminal connected to a first voltage level, whereby said PMOS transistor is permanently in an off state and draws a current proportionate to a difference of a voltage at said node and said first voltage level, wherein drawing of said current counters said leakage current.

[c64] 64. The counter_leakage circuit of claim 63, wherein said PMOS transistor is of a voltage specification of a second voltage level and said PMOS transistor is operated in an environment operating with input signals of said first voltage level, and said first voltage level is greater than said second voltage level.

[c65] 65. A counter_leakage circuit countering a leakage current, wherein said leakage current otherwise causes a voltage at a node to go beyond a desired voltage level, said counter_leakage circuit comprising:
a NMOS transistor having a drain terminal connected to said node, each of a source terminal and a gate terminal connected to a reference voltage level, whereby said NMOS transistor is permanently in an off state and draws

a current proportionate to a difference of a voltage at said node and said reference voltage level, wherein drawing of said current counters said leakage current.

[c66] 66. The counter_leakage circuit of claim 65, wherein said NMOS transistor is of a voltage specification of a second voltage level and said NMOS transistor is operated in an environment operating with a first voltage level, said first voltage level is greater than said second voltage level.

[c67] 67. A counter_leakage circuit countering a leakage current, wherein said leakage current otherwise causes a voltage at a node to go beyond a desired voltage level, said counter_leakage circuit comprising:
a transistor having a source terminal connected to said node and a gate terminal connected to receive a bias voltage, wherein said bias voltage is designed to turn on said transistor if the voltage at said node goes beyond said desired voltage; and
a current amplifier connected to a drain terminal of said transistor, wherein said current amplifier amplifies a current flowing through said transistor, whereby any leakage at said node is countered by current flow through said current amplifier.

[c68] 68. The counter_leakage circuit of claim 67, wherein said transistor is of a voltage specification of a second volt-

age level and said transistor is operated in an environment operating with a first voltage level, said first voltage level is greater than said second voltage level.

[c69] 69. The counter_leakage circuit of claim 68, wherein said transistor comprises an NMOS transistor having a drain terminal connected to a first voltage level and said NMOS transistor turns on if the voltage at said node is below (said bias voltage less a threshold voltage of said NMOS transistor).

[c70] 70. The counter_leakage circuit of claim 68, wherein said transistor comprises an PMOS transistor having a drain terminal connected to a reference voltage level and said PMOS transistor turns on if the voltage at said node is above (said bias voltage plus a threshold voltage of said PMOS transistor).

[c71] 71. A counter_leakage circuit countering a leakage current, wherein said leakage current otherwise causes a voltage at a node to go beyond a desired voltage level, said counter_leakage circuit comprising:
a set of diodes connected in series, wherein each of said set of diodes is designed such that the sum of cutting voltages of each of said set of diodes equals said desired voltage level, each of said set of diodes turns on if voltage at said first node goes beyond said desired voltage

level, whereby any leakage at said node is countered by current flow through said set of diodes.

[c72] 72. The counter_leakage circuit of claim 71, wherein each of said set of diodes is realized by a corresponding one of a set of transistors, wherein a drain terminal of each of said set of transistors is connected to a gate terminal of the same transistor, and a drain terminal of a first one of said set of transistors is connected to said node.

[c73] 73. The counter_leakage circuit of claim 72, wherein each of said set of transistors is of a voltage specification of a second voltage level and each of said set of transistors is operated in an environment operating with input signals of a first voltage level, wherein said first voltage level is greater than said second voltage level.

[c74] 74. The counter_leakage circuit of claim 73, wherein each of said set of transistors comprises a PMOS transistor, and a source terminal of a last one of said set of transistors is connected to said first voltage level.

[c75] 75. The counter_leakage circuit of claim 73, wherein each of said set of transistors comprises a NMOS transistor, and a source terminal of a last one of said set of transistors is connected to said reference voltage.

[c76] 76. A device comprising:
an input interface module providing an interface to receive an input signal having a swing equaling a second voltage level;
an output interface module providing an output signal on an output node;
a processing logic block comprising a protection circuit and a first transistor, said first transistor being of a voltage specification of a first voltage level, said first transistor and said protection circuit being designed to process information in said input signal, wherein said first voltage level is lower than said second voltage level, said protection circuit comprising:
a second PMOS transistor which switches to an off state if said input signal having said swing would cause a cross terminal voltage of said first transistor to exceed a permissible range, wherein said second PMOS transistor in said off state ensures that said cross terminal voltage of said first transistor does not exceed said permissible range.

[c77] 77. The device of claim 76, wherein said first transistor comprises a first PMOS transistor.

[c78] 78. The device of claim 77, wherein a source terminal of said first PMOS transistor being connected to a supply

voltage of said second voltage level.

[c79] 79. The device of claim 78, wherein said input signal swings between a reference voltage and said second voltage level.

[c80] 80. The device of claim 77, wherein said processing logic block further comprises a first NMOS transistor also of said voltage specification of said first voltage level, said protection circuit further comprising:
a second NMOS transistor which switches to an off state if said input signal would cause a cross terminal voltage of said first NMOS transistor to exceed a permissible range, wherein said second NMOS transistor in said off state ensures that said cross terminal voltage of said first NMOS transistor does not exceed said permissible range.

[c81] 81. The device of claim 80, wherein an upper limit of said permissible range equals an allowed maximum voltage associated with each of said first PMOS transistor and said first NMOS transistor.

[c82] 82. The device of claim 80, wherein each of said first PMOS transistor and said first NMOS transistor is contained in an input buffer, a drain terminal of each of said second PMOS transistor and said second NMOS transistor

being coupled to receive said input signal, a gate terminal of said second PMOS transistor being connected to receive a first bias voltage and a gate terminal of said second NMOS transistor being connected to receive a second bias voltage.

[c83] 83. The device of claim 82, said protection circuit further comprising:

a third PMOS transistor, a gate terminal of said third PMOS transistor being connected to said first bias voltage, a source terminal of said third PMOS transistor being connected to a gate terminal of said first PMOS transistor,

a drain terminal of said first PMOS transistor being connected to a source terminal of said second PMOS transistor, and a source terminal of said first PMOS transistor being connected to a supply voltage of said second voltage level,

wherein said third PMOS transistor ensures that a gate to source voltage (Vgs) and a gate to drain voltage (Vgd) of said first PMOS transistor from being exposed to voltage exceeding said permissible range.

[c84] 84. The device of claim 83, wherein said input buffer further comprises a fourth PMOS transistor, a gate terminal of said fourth PMOS transistor being connected to said source terminal of said second PMOS transistor, a

drain terminal of said fourth PMOS transistor connected to said source terminal of said third PMOS transistor, and a source terminal of said fourth PMOS transistor being connected to said supply voltage.

[c85] 85. The device of claim 84, wherein all of said first PMOS transistor, said second PMOS transistor, said third PMOS transistor, and said fourth PMOS transistor are of said voltage specification of said first voltage level.

[c86] 86. The device of claim 81, said protection circuit further comprising:
a third NMOS transistor, a gate terminal of said third NMOS transistor being connected to said second bias voltage, a source terminal of said third NMOS transistor being connected to a gate terminal of said first NMOS transistor,
a drain terminal of said first NMOStransistor being connected to a source terminal of said second NMOS transistor, and a source terminal of said first NMOStransistor being connected to a reference voltage,
wherein said third NMOS transistor ensures that a gate to source voltage (Vgs) and a gate to drain voltage (Vgd) of said first NMOStransistor from being exposed to voltage exceeding said permissible range.

[c87] 87. The device of claim 86, wherein said input buffer

further comprises a fourth NMOS transistor, a gate terminal of said fourth NMOS transistor being connected to said source terminal of said second NMOS transistor, a drain terminal of said fourth NMOS transistor connected to said source terminal of said third NMOS transistor, and a source terminal of said fourth NMOS transistor being connected to said reference voltage.

[c88] 88. The device of claim 87, wherein all of said first NMOStransistor, said second NMOS transistor, said third NMOS transistor, and said fourth NMOS transistor are of said voltage specification of said first voltage level.

[c89] 89. The device of claim 81, said first PMOS transistor and said first NMOS transistor being comprised in a logic gate, wherein each of said first NMOS transistor, said first PMOS transistor, said second NMOS transistor and said second PMOS transistor comprises a drain terminal, a source terminal and a gate terminal,
a gate terminal of said first NMOS transistor receiving a first swing signal and a gate terminal of said first PMOS transistor receiving a second swing signal, wherein each of said first swing signal and said second swing signal has a lower swing compared to a swing of said input signal but representing said information in said input signal,
wherein said gate terminal of said second PMOS transis-

tor is connected to a BIASP voltage, and said gate terminal of said second NMOS transistor is connected to a BIASN voltage,

said source terminal of said second PMOS transistor is connected to said drain terminal of said first PMOS transistor,

said source terminal of said first PMOS transistor is connected to a supply voltage of said second voltage level,

said drain terminal of said second PMOS transistor is connected to said drain terminal of said second NMOS transistor,

said source terminal of said second NMOS transistor is connected to said drain terminal of said first NMOS, and said source terminal of said first NMOS is connected to a reference voltage.

[c90] 90. The device of claim 89, wherein the drain terminal of said first PMOS transistor provides a first output signal having a swing equal to a swing of said first swing signal, the drain terminal of said first NMOS transistor provides a second output signal having a swing equal to a swing of said second swing signal, and the drain terminal of said second NMOS transistor provides a third output signal having a swing equal to a swing of said input signal, wherein each of said first output signal, said second output signal and said third output signal represents

an output of said logic gate.

[c91] 91. The device of claim 90, wherein said logic gate comprises an inverter.

[c92] 92. The device of claim 90, wherein said logic gate comprises a plurality of NMOS transistors including said first NMOS transistor, said logic gate also comprising a plurality of PMOS transistors including said first PMOS transistor, wherein a number of transistors in each of said plurality of NMOS transistors and said plurality of PMOS transistors equals a number of inputs to said logic gate.